PCS AMPLIFIER WITH INTEGRATED POWER CONTROL

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Abstract

A novel power control concept has been applied to a monolithic integrated power amplifier for the PCS / PCN frequency range of 1.9 to 2.4 GHz. At 3.3 V supply voltage the amplifier has a saturated power of 22.7 dBm at 1.95 GHz, which can be decreased continuously or in steps by an on chip control transistor. The amplifier has an efficiency better than 25% at P_{sat} and a gain of 25 dB at P_{-1dB}.

Introduction

For personal communication systems (PCS) power control of the transmit power amplifier becomes more and more important, especially in spread spectrum (CDMA) systems. The output power should be controllable over a range of 20-30 dB in steps or continuously. At the same time the power amplifier should have a high efficiency.
Conventionally power is controlled by lossy external switches or attenuators. This novel circuit proposed replaces the external components by using a MESFET as a variable control resistor in front of the final amplifier MESFET. The additional control MESFET has little influence on the overall performance of the power amplifier over a frequency range of 1.9 - 2.4 GHz. For comparison a power amplifier was designed without control on the same wafer.
The designed controllable power amplifier is comparable with power amplifiers without control reported in literature [1]. With a supply of 4.8 V an output power at the 1 dB compression point of 22.8 dBm at 1.9 GHz has been obtained in [2]. At the same frequency a power amplifier with 40.5 % efficiency and 22 dBm output power at 3.3 V supply is reported [3]. In a class A amplifier the second harmonic is suppressed by -33 dBc and the third by -40 dBc [4].

Power Control Concept

In Fig. 1 a block diagram of the power amplifier with power control is shown. The first two amplifier stages are conventional, consisting of transistors with gate widths of 300 µm and 600 µm. The third stage is the final power stage, consisting of a 3000 µm wide MESFET. This transistor is split into two

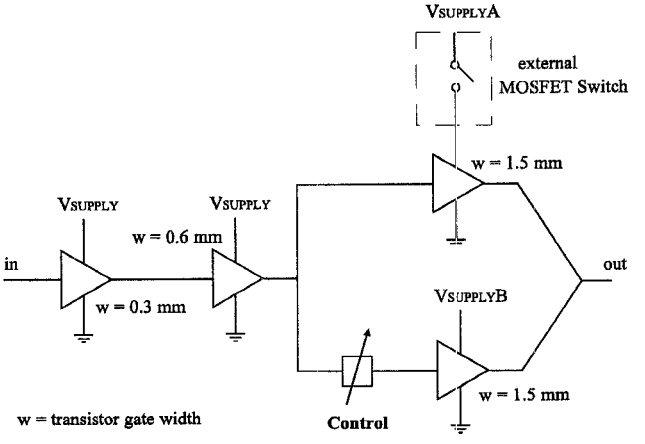

Fig.1: Block diagram of the power amplifier with power control

halves of 1500 µm each. All amplifier FETs have a threshold voltage of -0.6 V. The control transistor, a deep depletion MESFET with V_{th}=-2.0V, is placed in front of the gate of a 1500 µm transistor. With this control transistor half of the final stage can be almost completely isolated from the other half. To decrease DC power consumption, one of the final transistors can be switched off from the power supply $V_{supplyA}$

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by an external MOSFET switch. Using this switch, the total DC power consumption can be reduced by more than one third. The other half can be continuously regulated with the gate voltage of the control MESFET to decrease the output power further. The whole circuit was simulated with a harmonic balance simulator.

IC realization

The power amplifier was designed with a standard foundry MESFET process (Triquint QED/A). A gate length of 0.7 µm is used for all transistors except the power stage. The 2 x 1500 µm power transistors use a gate length of 0.8 µm allowing a finger width of 100 µm. The control FET is a 900 µm wide (12 x 75 µm) device. The schematic diagram is shown in Fig.2. The power amplifier is designed with an on chip input matching network. The first two stages

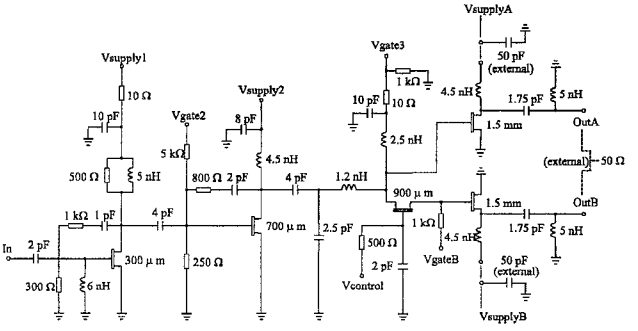

Fig.2: Schematic diagram

are stabilized with feedback. Those stages have a combined gain of approximately 18 dB. The output stage is designed conditionally stable. Due to the on chip high pass type output matching network the DC blocking is already included. It feeds two 100 Ω output pads in parallel.
The supply voltage is 3.3V. An external gate biasing of both final stage FETs is possible through on chip resistors. The layout (Fig. 3) is very compact with a chip size of 1 mm x 2 mm.

Measurements

Although the process is not a typical power process, the measured results show the excellent control performance of the designed power amplifier. On this wafer run a 0.8 µm MESFET has a saturation current of I_{dss} = 45 mA/mm. A supply voltage of 3.3V and a frequency of 1.95 GHz are used for the measurements discussed below.

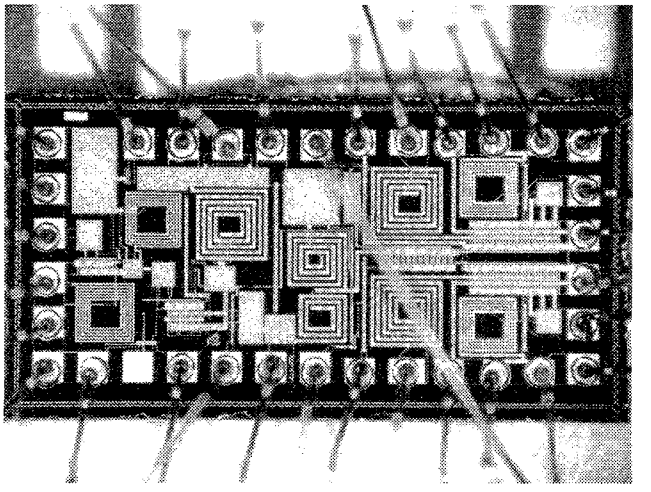

Fig.3: Photo of the controllable power amplifier

For comparison a power amplifier was designed without the controlling stage. In Fig. 4 the power characteristic of the fundamental, second and third harmonic is shown for the power amplifier with control transistor (C) and the normal one without the control (N). The normal power amplifier has more saturated power, 23.6 dBm, than the controlled power amplifier with $V_{control}$ = 0 V, 22.7 dBm. The control transistor reduces the maximum output

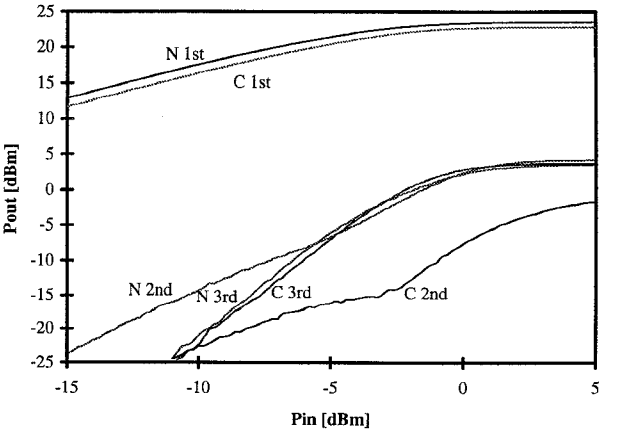

Fig.4: Comparison of the harmonics of the power amplifier without (N) and with (C) the control transistor ($V_{control}$ = 0 V)

capability by less than 1 dB. The linear gain is 27.5 dB for the normal power amplifier and 26.4 dB for the controlled one.

The second harmonic is remarkably different. The normal amplifier has relative harmonic suppression of 19 dBc at full compression. In comparison the power amplifier with control has 24 dBc. Thus, the control transistor decreases the level of the second harmonic by 5 dB. The third harmonic is similar for both designs. The suppression is 19.5 dBc and 19.0 dBc for the normal and the controlled amplifier respectively.

Fig. 5 shows the output power vs input power with the control voltage as a parameter. The output power can be continuously controlled by the voltage

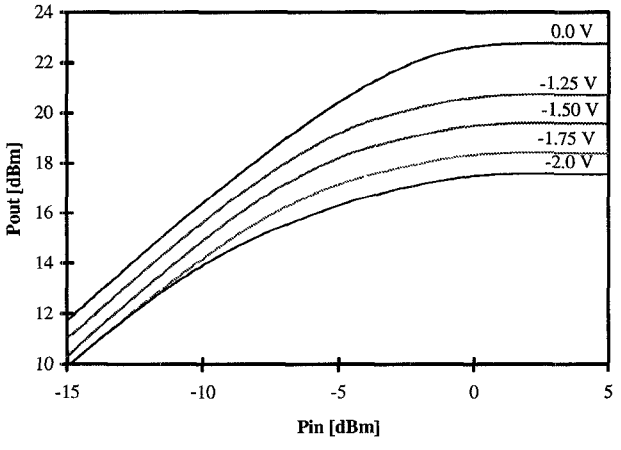

Fig.5: Measured output power vs input power as a function of $V_{control}$ ($V_{supplyA}$ and $V_{supplyB}$ connected)

applied to the control transistor. With increasing control voltage the 1 dB compression points move to lower values. An almost pinched-off control transistor $V_{control}$ = -2.0 V results in a saturated power of 17.5 dBm.

The saturated power P_{sat} and the output power P_{-1dB} versus $V_{control}$ is shown in Fig. 6. The maximum P_{-1dB} with $V_{control}$ = 0 V is 21 dBm. If the drain-source channel of the control transistor is opened further with a positive voltage, the output power will remain almost constant. This indicates a nearly lossless control at $V_{control}$ = 0 V. The overall power added efficiencies at different control voltages are also shown. At $V_{control}$ = 0 V the power amplifier has an overall efficiency better than 25%.

When the upper half of the power stage is disconnected from the supply voltage, the power versus $V_{control}$ characteristic of Fig. 7 is measured. At $V_{control}$ = 0 V the output power is 17 dBm with an overall efficiency of 14%. At $V_{control}$ = -2.5 V the output power is -4.6 dBm. The maximum power control range, shown in Fig. 5 and 7, exceeds 25 dB.

In Fig. 8 the output power versus frequency as a function of input power is shown. When both halves of the final power stage (B) are connected to the

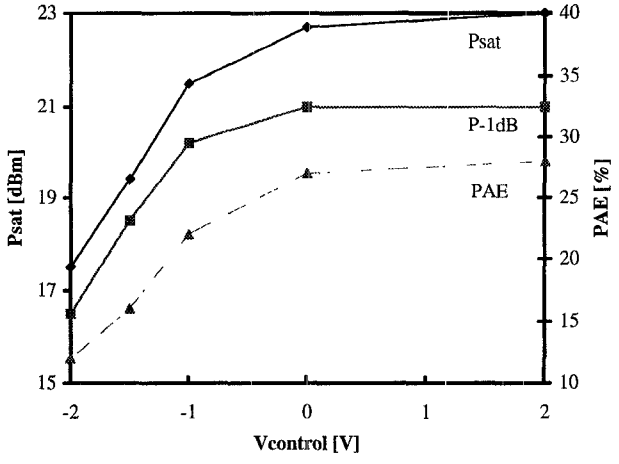

Fig.6: P_{sat}, P_{-1dB} and overall power added efficiency (PAE) at saturation as a function of $V_{control}$

supply voltage, the output power varies less than 1dB over the frequency range of 1.9 - 2.4 GHz. While decreasing control voltage to $V_{control}$ = -2.0 V, the output power becomes smoother over a wider frequency range. When only a single power transistor (S) is connected to the supply voltage, an increasing slope of the output power with decreasing control voltage is obvious. In the frequency range of 1.9 - 2.4 GHz, the maximum gain variation is 4 dB with applied control voltage.

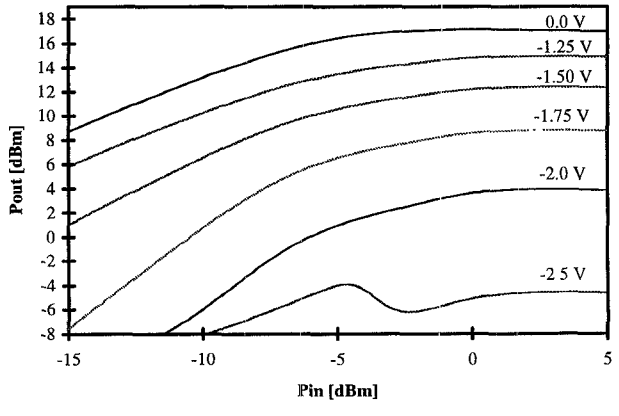

Fig.7: Measured output power vs input power as a function of $V_{control}$ for $V_{supplyA}$ disconnected

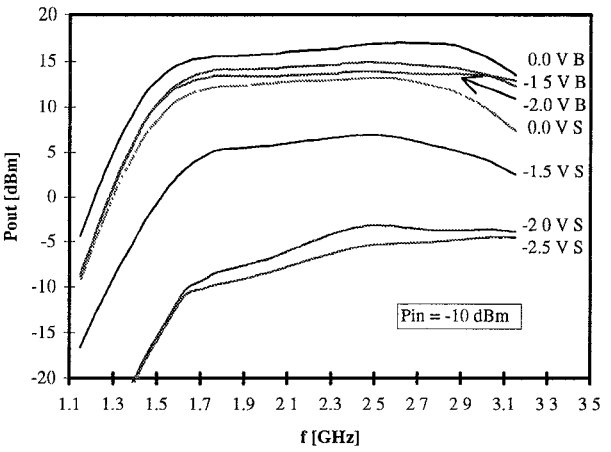

Fig.8: P_{out} vs frequency for P_{in} = -10 dBm as a function of $V_{control}$ (B: $V_{supplyA}$ and $V_{supplyB}$ is connected; S: $V_{supplyA}$ is disconnected and $V_{supplyB}$ is connected)

Conclusions

A power amplifier with on-chip integrated power control was designed for the frequency range of 1.9 - 2.4 GHz. With a supply voltage of 3.3 V an output power of 22.7 dBm and a gain of 25 dB was measured at 1.95 GHz. The output power can be controlled continuously or in steps by an on-chip control over more than 25 dB.

Acknowledgment

We are grateful to our colleague M. Lanz for packaging the circuits in the test fixtures.

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